thus causing a corresponding drop in voltage. As the output voltage drops, the current-limit threshold also drops fractionally. The result is a decreasing output current as the voltage decreases; the limit is 0.2A at 1V of output. This foldback effect reduces power dissipation in the control device, which lets you use simple heat sinking.

When operating from a 6V raw supply, the rail-to-rail output drive from IC_{1B} can produce the full gate-source voltage and fully enhance (turn on) the PMOS transistor. The dropout voltage is 0.2V at 500 mA and 0.6V at 1A.

4- to 20-mA loop circuits

Amplifiers whose outputs swing close to the negative rail enhance and simplify the design of 4- to 20-mA loop transmitters. Amplifiers that can't swing close to this rail have saturation-voltage limits that reduce the accuracy of the amp's zero-scale signal range. The output—and many times the input—of an amplifier often operates at or near the negative rail, yet the amplifier must remain linear. A case in point is the circuit in **Fig 5**, a loop-powered strain-gauge sensor. The amplified 50-mV full-scale (FS) bridge output is calibrated for a 4- to 20-mA transmitter output.

IC_1 linearly amplifies the bridge signal by a gain of about 40. IC_1's output range includes the negative rail, so the IC can amplify a 0- to 50-mV bridge signal to 0 to 2.008V referred to the loop's common bus (pin 5 of IC_1). Because all negative-supply device pins refer to this point, the bulk of the loop's quiescent current flows into R_6 and the external loop and termination, R_{LOAD}.

With no output from the bridge, IC_1's output will be at the negative rail. No current flows through R_1 or R_2 into the summing point of IC_2 because IC_1 servos the summing point to the negative-rail potential. For this zero-scale signal condition, R_3 (4-mA NULL) calibrates the loop for a 4-mA output current or for 0.4V across R_{LOAD}. Because no current flows through R_1 in this zero-scale condition, R_1 has no effect on nulling, which ensures that the NULL and SPAN trims don't interact.

R_3 and R_4 effectively appear across the 5V reference output, so the current the reference injects into the loop is constant. The loop's output summing resistors, R_5 and R_6, scale the current. The expression for this current is

$$I_{NULL} \approx \left(\frac{5V}{R_3+R_4}\right)\left(1+\frac{R_5}{R_6}\right),$$

where 5V represents IC_3's reference voltage.

When the bridge output is 50 mV FS, IC_1 amplifies the output to the 2.008V FS level and supplies signal current to IC_2's summing point. Like the reference current through R_3 and R_4, the loop scales up the signal current in R_1 and R_2. The current appears

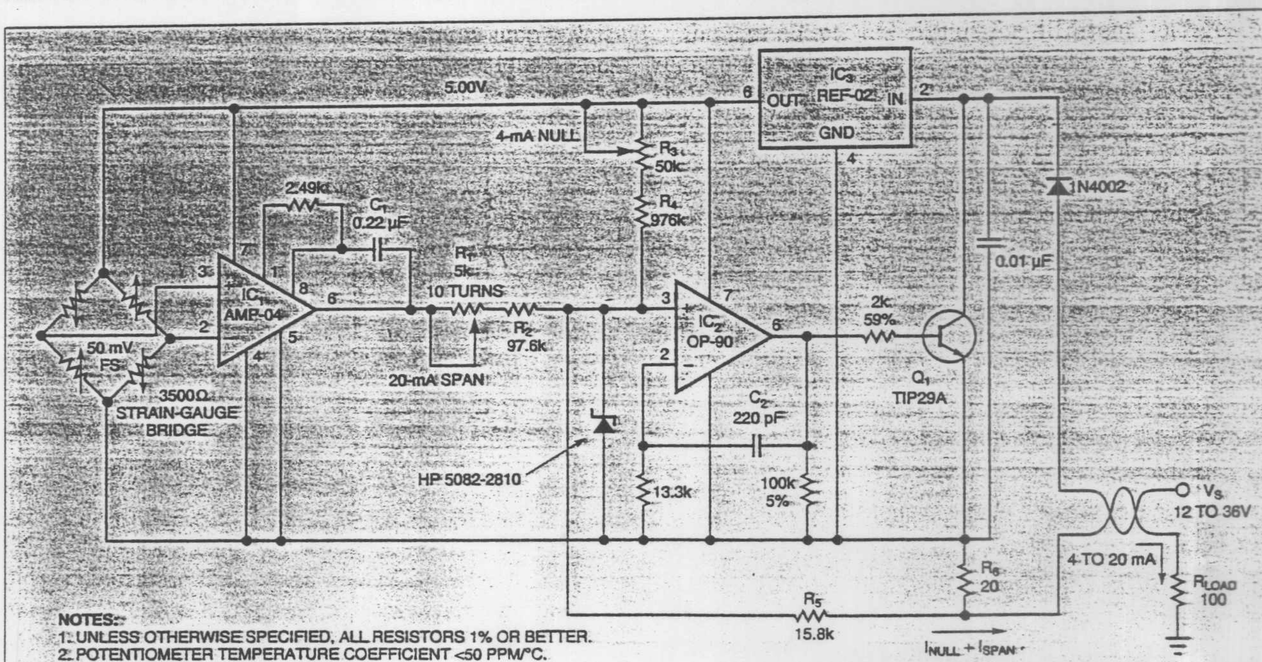

Fig 5—Single-supply amplifiers enhance the design of 4- to 20-mA current loops—such as this circuit, which features noninteractive trims—because the amplifiers can swing close to the negative rail and accurately amplify zero-scale signals.

through R_6 as I_{SPAN}:

$$I_{SPAN} \approx \left(\frac{V_{BRIDGE} \times A}{R_1 + R_2}\right)\left(1 + \frac{R_5}{R_6}\right),$$

where V_{BRIDGE} is the output of the bridge, and A is IC_1's gain. For a 50-mV FS bridge output, R_1 (20-mA SPAN) trims the circuit for a 20-mA output current (4-mA I_{NULL} plus 16-mA I_{SPAN}) or 2V across R_{LOAD}.

In this circuit, the three active devices and the 3500Ω bridge draw 3.75 mA worst case, which is safely below the system's 4-mA zero scale. C_1 provides a 7-Hz lowpass filter to limit noise, and C_2 stabilizes IC_2's output loop. Q_1, a TO-220 device, conducts the 0- to 16-mA I_{SPAN} portion of the loop output.

Most DACs require dual supplies. Among those that don't, most work from 12 to 15V supplies, as opposed to 5V only. This situation greatly reduces your component choices for single 5V-supply systems. CMOS R/2R-ladder DACs are natural choices for low-voltage operation because many of these units work from 5V supplies. However, when you use DACs in their standard multiplying mode with a positive reference and an inverting-output amplifier, the DACs also require a negative supply so the amplifier can output negative voltages. Or, conversely, if you use a negative reference, the output will be positive. In either case, you will need a negative supply.

To make such a DAC operate in a totally unipolar fashion, you can turn it around and operate it in what is known as its inverted, or voltage-output, mode. In **Fig 6**, the DAC's standard V_{REF} input to the ladder becomes the voltage-output node (pin 1), and the normal I_{OUT} node becomes the reference input (pin 3). This voltage-output-mode CMOS DAC circuit works from 5V using two 8-pin ICs to achieve serial-input 12-bit operation. The DAC produces a 0 to 4.095V output (1 mV/LSB).

The circuit uses a 12-bit multiplying DAC, so the output voltage equals $(D \div 4096) \times V_{REF}$, where D is the 12-bit digital word's value, which ranges from 0 to 4095. With a 1.235V V_{REF}, the unbuffered output at pin 1 of IC_1 will be $(4095 \div 4096) \times 1.235V$ at full scale, or approximately 1.2347V (~300 μV/LSB). The output amplifier brings the overall scale at V_{OUT} to the $(D \div 4096) \times V_{REF} \times A$ level, where A is the amplifier gain. With the appropriate choice of A, the output will be 1 mV/LSB. The amplifier gain required for this weighing is about 3.3. The gain is variable (see R_2 and R_3), so you can trim out tolerances in both the reference voltage and gain resistors. For bipolar amplifiers, making the equivalent resistance of the gain divider equal to the DAC's output resistance of 11 kΩ proves helpful.

The circuit is clean and straightforward, but some application points are worth discussion. Note that the enhancement voltage of the DAC's internal NMOS

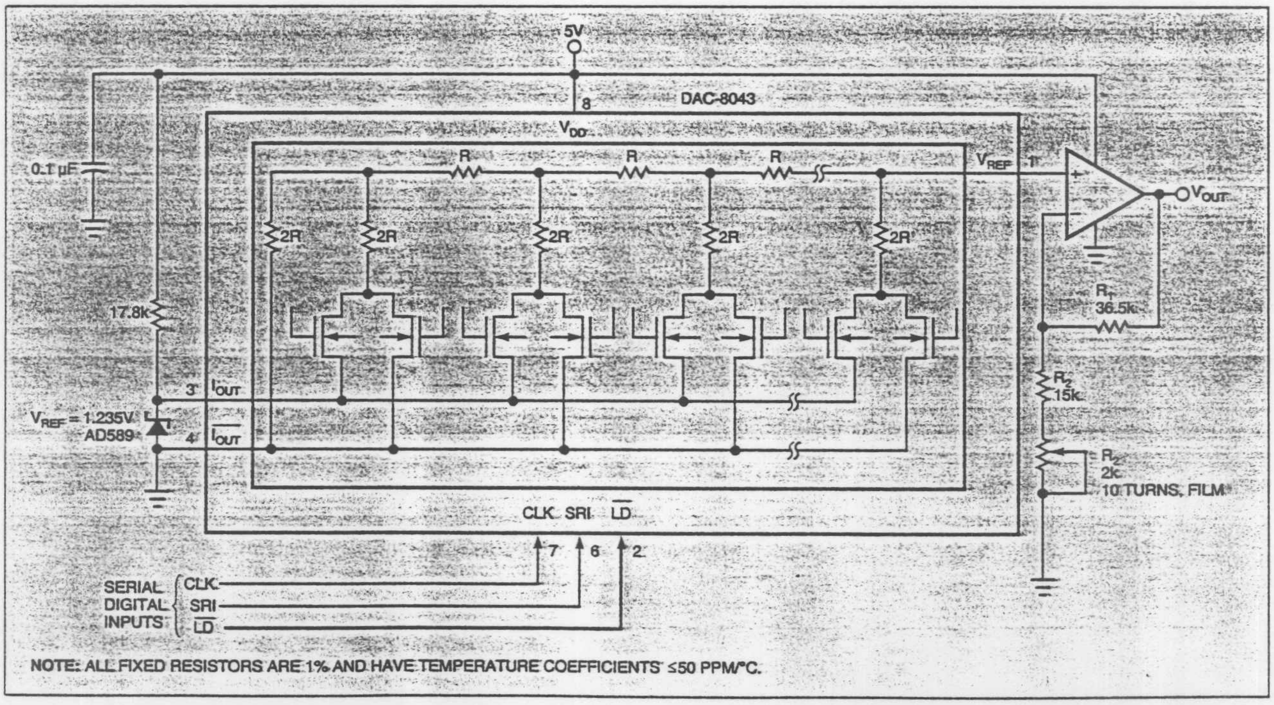

Fig 6—To run a standard CMOS R/2R-ladder DAC from a single supply, you have to operate the DAC in the inverted, or voltage-output, mode.